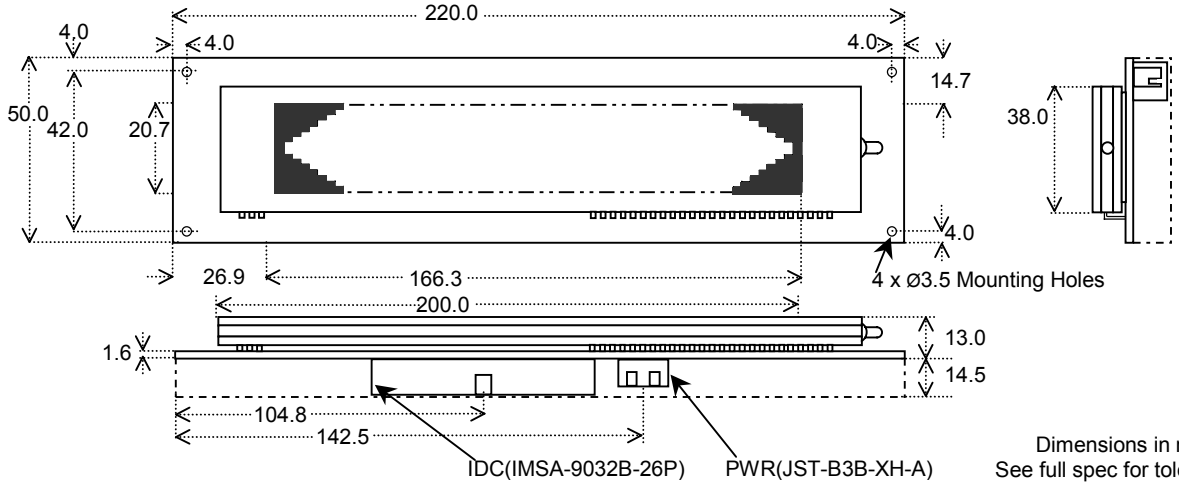
Dot Graphic VFD Module — GU256X32-800

- **256 x 32 Dot Graphic**
- **Operating Temp -40°C to +85°C**
- **Single 5V Supply.**
- **High Brightness Blue Green Display**
- **Selectable Parallel (i80/M68)/Serial Interface**
- **Twin Screen Graphic RAM**
- **16 Level Brightness Control Function**

The module includes the Vacuum Fluorescent Display glass, driver and control ASIC, with integral refresh Graphic RAM and logic for parallel and synchronous serial interfaces. The high speed 8 bit parallel interface is 5V CMOS compatible suitable for connection to a host CPU bus. Brightness control and power down functions are provided. A full data sheet is available.



Dimensions in mm
See full spec for tolerances

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Condition
Power Supply Voltage	V_{CC}	5.0VDC +/- 5%	GND=0V
Power Supply Current	I_{CC}	750mADC typ.	V_{CC}= 5V
Logic High Input	V_{IH}	0.8Vcc VDC min.	I_{IH} = 2uA
Logic Low Input	V_{IL}	0.2Vcc VDC max.	I_{IL} = -600uA
Logic High Output	V_{OH}	Vcc-0.3 VDC min.	I_{OH} = -300uA
Logic Low Output	V_{OL}	0.3 VDC max.	I_{OL} = 300uA

The power on rise time should be less than 100ms.The inrush current at power on can be 2 x I_{CC}.

OPTICAL and ENVIRONMENTAL SPECIFICATIONS

Parameter	Value
Display Area (XxY mm)	166.25 x 20.65
Dot Size/Pitch (XxY mm)	0.5 x 0.5/0.65 x 0.65
Luminance	250 cd/m^2 Min.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +85°C
Operating Humidity (non condensing)	20 to 80% RH @ 25°C

SOFTWARE COMMANDS

Instruction	C/$\overline{D}$	Instruction Byte	No. Bytes
Set Display On/Off / Layer Merge	1	20H→2FH	2
Set Display Brightness	1	40H→4FH	1
Clear Display	1	52H→5FH	1
Set Cursor XY Address	1	60H→67H	3
Set Display Start X Address	1	70H→7FH	2
Set Write Address Mode	1	80H→8FH	1
Scroll Display Vertically Up/Down	1	B0H→BFH	1
Read Data At XY Address	1	D4H→D7H	3
Write Data	0	00H→FFH	1

TIMING PARAMETERS (min)

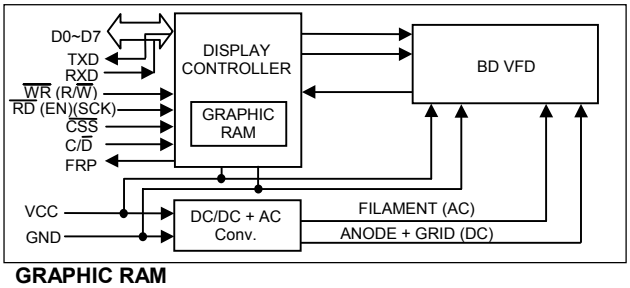
i80/M68 Parameters	Time
Write $\overline{WR}$/EN Cycle Time	750ns
Write $\overline{WR}$/EN Pulse Width	100ns
Hold after Write $\overline{WR}$/EN	30ns
Set Up To Write $\overline{WR}$/EN	30ns

Serial Parameters	Time
SCK Cycle Time	500ns
SCK Pulse Width	200ns
Delay After 8th bit, $\overline{CSS}$="L"	150ns
Set Up To SCK, $\overline{CSS}$="L"	60ns

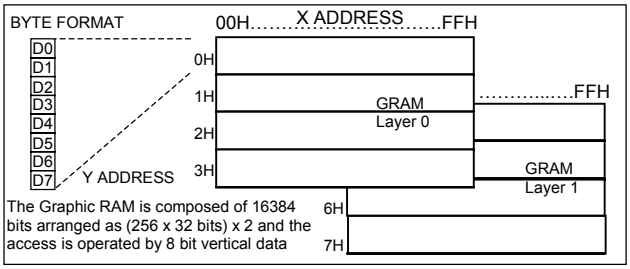
SCROLLING GRAPHIC DISPLAY

The pattern in GRAM can be scrolled around the display. Horizontal scroll is achieved by increment/decrement of the Display Start X Address. The vertical scroll process considers layer 0, then layer 1 as a continuous 64 bit high vertical area within RAM.

BLOCK DIAGRAM



GRAPHIC RAM



The Graphic RAM is composed of 16384 bits arranged as (256 x 32 bits) x 2 and the access is operated by 8 bit vertical data

IDC DATA CONNECTOR

Pin	i80	M68	Serial	Pin	Sig
1	D7	D7	X	2	GND
3	D6	D6	X	4	GND
5	D5	D5	X	6	GND
7	D4	D4	X	8	GND
9	D3	D3	X	10	GND
11	D2	D2	X	12	GND
13	D1	D1	SO	14	GND
15	D0	D0	SI	16	GND
17	$\overline{WR}$	R/$\overline{W}$	X	18	GND
19	C/$\overline{D}$	C/$\overline{D}$	C/$\overline{D}$	20	GND
21	$\overline{RD}$	EN	SCK	22	GND
23	$\overline{CSS}$	$\overline{CSS}$	$\overline{CSS}$	24	GND
25	FRP	FRP	FRP	26	/RES

3 PIN POWER CONNECTOR

Pin	Sig
1	Vcc
2	Test (Factory only)
3	GND

PCB JUMPERS (O)pen (L)ink

Interface	J1	J2
Serial	L	O / L
i80 Parallel	O	L
M68 Parallel	O	O

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